WHAT IS CLAIMED IS:

1. A method of using a software tool to analyze a VLSI circuit, the method comprising:

prior to initiating analysis of the circuit, performing a complexity check on the circuit;

responsive to the circuit failing the complexity check, aborting analysis of the circuit; and

responsive to the circuit passing the complexity check:

initiating analysis of the circuit; and

continuing analysis of the circuit until expiration of a predetermined time period following the initiating.

2. The method of claim 1 further comprising, upon expiration of the predetermined time period, halting analysis of the circuit.

3. The method of claim 2 further comprising, responsive to the halting, saving data generated during the analysis.

4. The method of claim 1 wherein the performing a complexity check comprises determining whether a number of transistors comprising the circuit exceeds a preselected threshold value.

5. The method of claim 1 wherein the performing a complexity check comprises determining whether a number of possible logical paths through the circuit exceeds a preselected threshold value.

6. The method of claim 1 wherein the initiating analysis of the circuit further comprises setting a timer to time out upon expiration of a predetermined time period.

7. The method of claim 6 wherein the continuing analysis further comprises continuing analysis of the circuit until the timer times out.

8. The method of claim 1 wherein the initiating analysis of the circuit comprises initiating a process for verifying reliable operation of the circuit.

9. A computer-implemented tool for analyzing a VLSI circuit, comprising:

means for performing a complexity check on the circuit prior to initiating analysis thereof;

means responsive to the circuit failing the complexity check for aborting analysis of the circuit;

means responsive to the circuit passing the complexity check for initiating analysis of the circuit; and

means for continuing the analysis for a predetermined time period.

10. The computer-implemented tool of claim 9 further comprising means for halting analysis of the circuit upon expiration of the predetermined time period.

11. The computer-implemented tool of claim 10 further comprising means responsive to the halting for saving data generated during the analysis.

12. The computer-implemented tool of claim 9 wherein the means for performing a complexity check comprises means for determining whether a number of transistors of the circuit exceeds a preselected threshold value.

13. The computer-implemented tool of claim 9 wherein the means for performing a complexity check comprises means for determining whether a number of possible logical paths through the circuit exceeds a preselected threshold value.

14. The computer-implemented tool of claim 9 wherein the means for initiating analysis of the circuit further comprises means for setting a timer to time out upon expiration of a predetermined time period.

15. The computer-implemented tool of claim 14 wherein the means for continuing analysis of the circuit further comprises means for continuing analysis of the circuit until the timer times out.

16. The computer-implemented tool of claim 9 wherein the means for initiating analysis of the circuit comprises means for initiating a process to verify reliable operation of the circuit.

17. A computer-readable medium operable with a computer to analyze a VLSI circuit, the medium having stored thereon:

instructions executable by the computer for performing a complexity check on the circuit prior to initiating analysis thereof;

instructions executable by the computer responsive to the circuit failing the complexity check for aborting analysis of the circuit; and

instructions executable by the computer responsive to the circuit passing the complexity check for initiating analysis of the circuit and continuing analysis of the circuit until expiration of a predetermined time period following the initiating.

18. The computer-readable medium of claim 17 further having stored thereon instructions executable by the computer for halting analysis of the circuit upon expiration of the predetermined time period.

19. The computer-readable medium of claim 18 further having stored thereon instructions executable by the computer responsive to the halting for saving data generated during the analysis.

20. The computer-readable medium of claim 17 wherein the instructions for performing a complexity check comprise instructions for determining whether a number of transistors comprising the circuit exceeds a preselected threshold value.

21. The computer-readable medium of claim 17 wherein the instructions for performing a complexity check comprise instructions for determining whether a number of possible logical paths through the circuit exceeds a preselected threshold value.

22. The computer-readable medium of claim 17 wherein the instructions for initiating and continuing analysis of the circuit further comprise instructions for setting a timer to time out upon expiration of a predetermined time period.

23. The computer-readable medium of claim 22 wherein the instructions for initiating and continuing analysis of the circuit further comprise instructions for continuing analysis of the circuit until time out of timer.

24. The computer-readable medium of claim 17 wherein the instructions for initiating analysis of the circuit comprises instructions for initiating a process to locate one or more areas of the circuit that suffer at least one of electromigration and self-heating.